Advanced Non-Volatile Memories (NVM)

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Open Access

Acronyms

Acronym	Definition
1MB	1 Megabit
3D	Three Dimensional
3DIC	Three Dimensional Integrated Circuits
ACE	Absolute Contacting Encoder
ADC	Analog to Digital Converter
AEC	Automotive Electronics Council
AES	Advanced Encryption Standard
AF	Air Force
AFRL	Air Force Research Laboratory
AFSMC	Air Force Space and Missile Systems Center
AMS	Agile Mixed Signal
ARM	ARM Holdings Public Limited Company
BGA	Ball Grid Array
BOK	Body of Knowledge
CAN	Controller Area Network
CBRAM	Conductive Bridging Random Access Memory
CCI	Correct Coding Initiative
CGA	Column Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CN	Xilinx ceramic flip-chip (CF and CN) packages are ceramic column grid array (CCGA) packages
COTS	Commercial Off The Shelf
CRC	Cyclic Redundancy Check
CRÈME	Cosmic Ray Effects on Micro Electronics
CRÈME MC	Cosmic Ray Effects on Micro Electronics Monte Carlo
CSE	Crypto Security Engin
CU	Control Unit
D-Cache	defered cache
DCU	Distributed Control Unit
DDR	Double Data Rate (DDR3 = Generation 3; DDR4 = Generation 4)
DLA	Defense Logistics Agency
DMA	Direct Memory Access
DMEA	Defense MicroElectronics Activity
DoD	Department of Defense
DOE	Department of Energy
DSP	Digital Signal Processing
dSPI	Dynamic Signal Processing Instrument
Dual Ch.	Dual Channel
ECC	Error-Correcting Code
EEE	Electrical, Electronic, and Electromechanical
EMAC	Equipment Monitor And Control
EMIB	Multi-die Interconnect Bridge
ESA	European Space Agency
eTimers	Event Timers
ETW	Electronics Technology Workshop
FCCU	Fluidized Catalytic Cracking Unit
FeRAM	Ferroelectric Random Access Memory
FinFET	Fin Field Effect Transistor (the conducting channel is wrapped by a thin silicon "fin")
FPGA	Field Programmable Gate Array
FPU	Floating Point Unit
FY	Fiscal Year
GaN	Gallium Nitride
GAN GIT	Panasonic GaN GIT Eng Prototype Sample
GAN SIT	Gallium Nitride GIT Eng Prototype Sample
Gb	Gigabyte
GCR	Galactic Cosmic Ray
GIC	Global Industry Classification

Acronym	Definition
Gov't	Government
GPU	Graphics Processing Unit
GRC	NASA Glenn Research Center
GSFC	Goddard Space Flight Center
GSN	Goal Structured Notation
GTH/GTY	Transceiver Type
HALT	Highly Accelerated Life Test
HAST	Highly Accelerated Stress Test
HBM	High Bandwidth Memory
HDIO	High Density Digital Input/Output
HDR	High-Dynamic-Range
HiREV	High Reliability Virtual Electronics Center
HMC	Hybrid Memory Cube
HP Labs	Hewlett-Packard Laboratories
HPIO	High Performance Input/Output
HPS	High Pressure Sodium
HUPTI	Hampton University Proton Therapy Institute
I/F	interface
I/O	input/output
I2C	Inter-Integrated Circuit
i2MOS	Microsemi second generation of Rad-Hard MOSFET
IC	Integrated Circuit
IC	Integrated Circuit
I-Cache	independent cache
IUCF	Indiana University Cyclotron Facility
JFAC	Joint Federated Assurance Center
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (FPGAs use JTAG to provide access to their programming debug/emulation functions)
KB	Kilobyte
L2 Cache	independent caches organized as a hierarchy (L1, L2, etc.)
LANL	Los Alamos National Laboratories
LANSCE	Los Alamos Neutron Science Center
LLUMC	Loma Linda University Medical Center
L-mem	Long-Memory
LP	Low Power
LVDS	Low-Voltage Differential Signaling
LW HPS	Lightwatt High Pressure Sodium
M/L BIST	Memory/Logic Built-In Self-Test
MBMA	Model-Based Missions Assurance
MGH	Massachusetts General Hospital
Mil/Aero	Military/Aerospace
MIPI	Mobile Industry Processor Interface
MMC	MultiMediaCard
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MP	Microprocessor
MP	Multiport
MPFE	Multiport Front-End
MPU	Microprocessor Unit
Msg	message
NAND	Negated AND or NOT AND
NASA	National Aeronautics and Space Administration
NASA STMD	NASA's Space Technology Mission Directorate
Navy Crane	Naval Surface Warfare Center, Crane, Indiana
NEPP	NASA Electronic Parts and Packaging
NGSP	Next Generation Space Processor
NOR	Not OR logic gate

Acronym	Definition
NRL	Naval Research Laboratory
NRO	United States Navy National Reconnaissance Office
NSWC Crane	Naval Surface Warfare Center, Crane Division
OCM	On-chip RAM
PBGA	Plastic Ball Grid Array
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCIe Gen2	Peripheral Component Interconnect Express Generation 2
PLL	Phase Locked Loop
POL	point of load
PoP	Package on Package
PPAP	Production Part Approval Process
Proc.	Processing
PS-GTR	High Speed Bus Interface
QDR	quad data rate
QFN	Quad Flat Pack No Lead
QSPI	Serial Quad Input/Output
R&D	Research and Development
R&M	Reliability and Maintainability
RAM	Random Access Memory
ReRAM	Resistive Random Access Memory
RGB	Red, Green, and Blue
RH	Radiation Hardened
SATA	Serial Advanced Technology Attachment
SCU	Secondary Control Unit
SD	Secure Digital
SD/eMMC	Secure Digital embedded MultiMediaCard
SD-HC	Secure Digital High Capacity
SDM	Spatial-Division-Multiplexing
SEE	Single Event Effect
SESI	secondary electrospray ionization
Si	Silicon
SiC	Silicon Carbide
SK Hynix	SK Hynix Semiconductor Company
SLU	Saint Louis University
SMDs	Selected Item Descriptions
SMMU	System Memory Management Unit
SNL	Sandia National Laboratories
SOA	Safe Operating Area
SOC	Systems on a Chip
SPI	Serial Peripheral Interface
STT	Spin Transfer Torque
TBD	To Be Determined
Temp	Temperature
THD+N	Total Harmonic Distortion Plus Noise
TRIUMF	Tri-University Meson Facility
T-Sensor	Temperature-Sensor
TSMC	Taiwan Semiconductor Manufacturing Company
U MD	University of Maryland
UART	Universal Asynchronous Receiver/Transmitter
UFHPTI	University of Florida Proton Health Therapy Institute
UltraRAM	Ultra Random Access Memory
USB	Universal Serial Bus
VNAND	Vertical NAND
WDT	Watchdog Timer

Outline

- Introduction – Purpose & Priorities
- Roadmap
- Technology Evaluation and Test Results
  - ReRAM
  - STT-MRAM
  - 3D NAND Flash
- Upcoming Tests & Future Plans
- Summary

NEPP – Memories

New materials/ architectures
- Resistive
  - Fujitsu/Panasonic
- Spin torque transfer magnetoresistive
  - Avalanche, Everspin
- 3D Xpoint
  - Intel Optane
- Enabling “universal” memories

DRAMs
- DDR4 test capability (in progress)
- Commercial DDR (various)
- Tezzaron DiRAM
- Enabling high performance computing

Commercial Flash
- 3D
  - Samsung, Hynix, Micron
- Planar – TBD
- Enabling data storage density

Partnering
- Navy Crane
- NASA STMD
- Avalanche
- University of Padova

Best Practices and Guidelines

Related task areas:

Deprocessing for single event testing (also w/processors, FPGAs,…)

Commercial NVM Technology Roadmap

- collaborative with NSWC Crane, others

Other

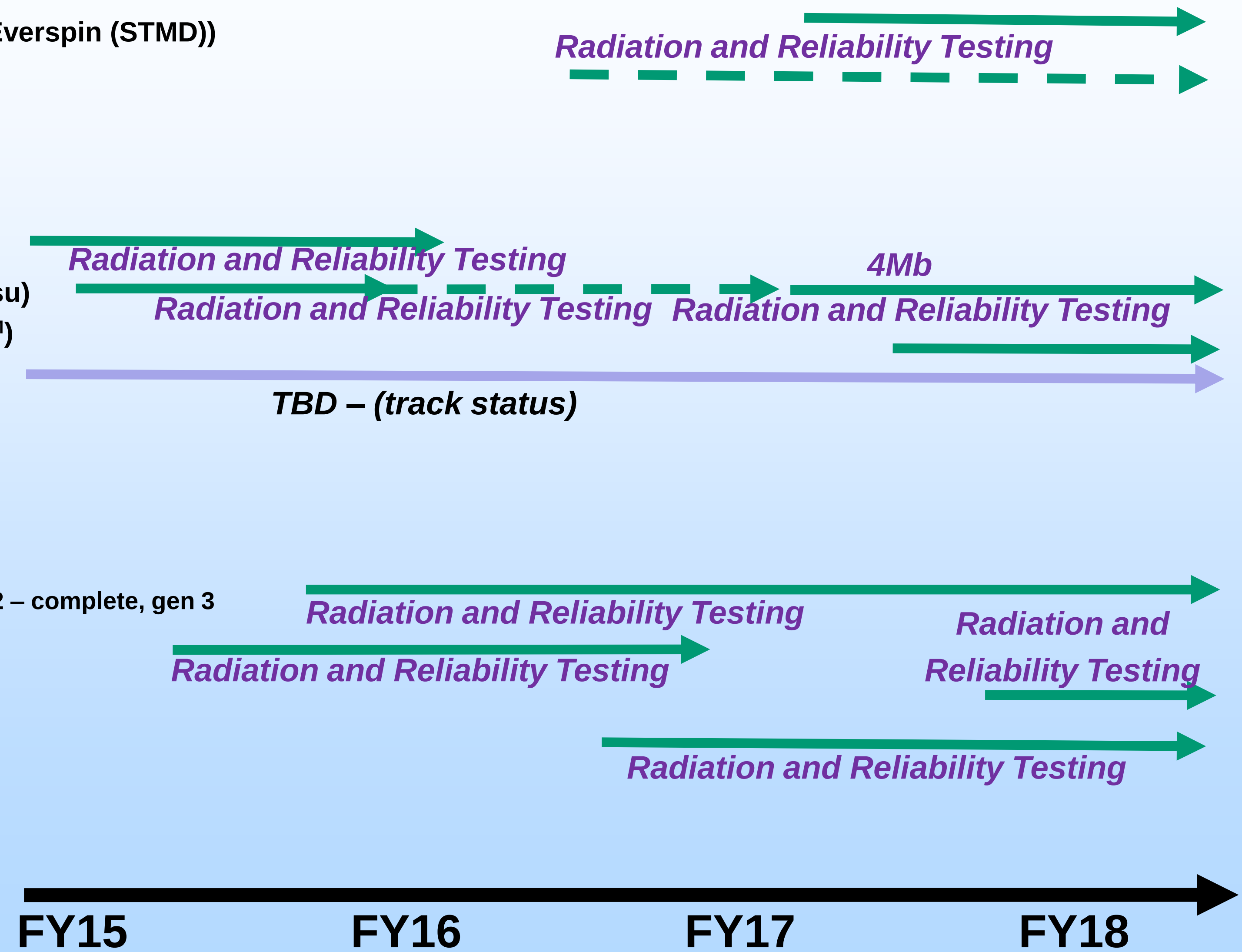
- STT-MRAM (Avalanche, Everspin (STMD))
- FeRAM

Resistive

- CBRAM (Adesto)
- ReRAM (Panasonic/Fujitsu)
- 3D XPoint (Intel Optane™)
- TBD (HP Labs, others)

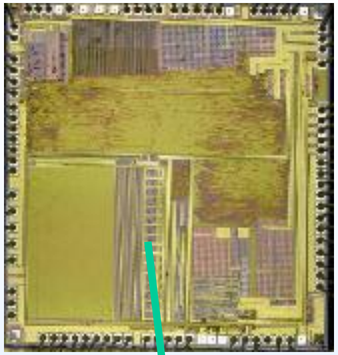
NAND FLASH

- Samsung VNAND (gen 1, 2 – complete, gen 3 FY17)
- Micron 16nm planar
- Micron 3D
- SK Hynix 3D, other



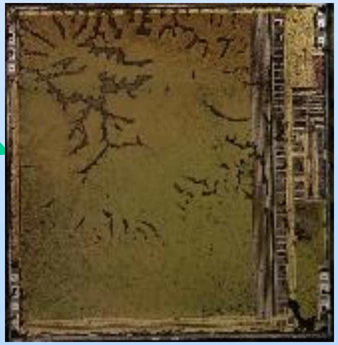
Resistive Memory (ReRAM)

- Resistive Memory is a Long Term Storage Candidate Technology
  - Inherently TID-hard memory elements (Sandia, HP labs, etc)
  - Potential for high density storage memory
- Panasonic Embedded ReRAM
  - 512Kb embedded in microcontroller tested 2015/16
  - Pulsed laser testing shows robust cells - but sensitivity in the sense amps
  - Memory reliability similar or better than flash
- Fujitsu/Panasonic ReRAM
  - 4Mb stand-alone ReRAM chip
  - Memory cell tech node same as previous embedded memory, but configured for high endurance with EDAC
  - Of interest to understand density scaling of ReRAM without microcontroller
    - Future 45 and 14nm planned by Fujitsu



Panasonic Embedded ReRAM

Location of pulsed laser bit upset sensitivity marked "1"

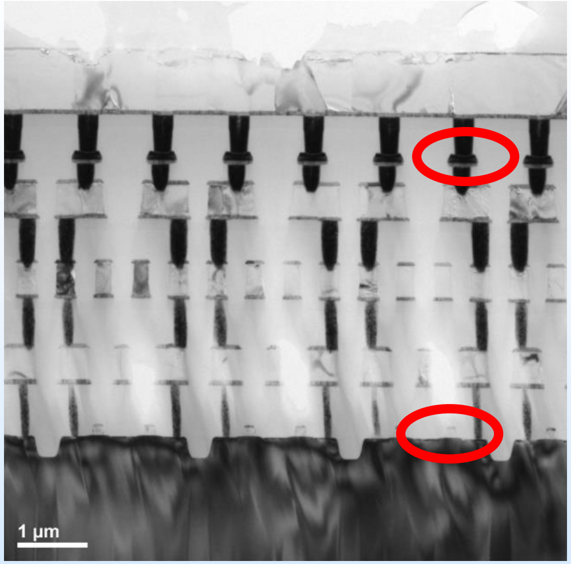


Fujitsu ReRAM

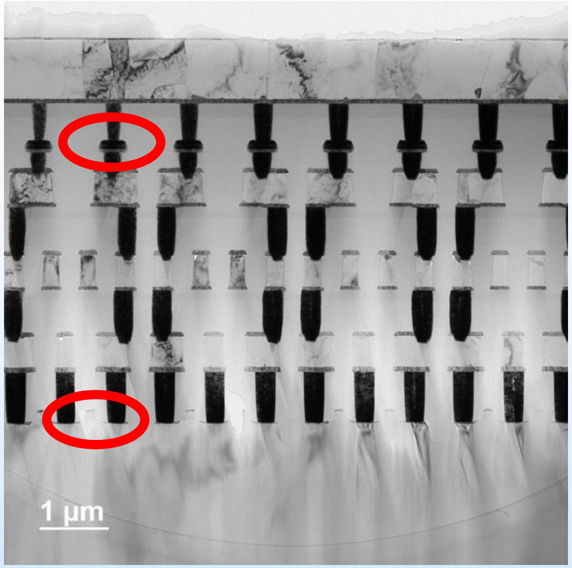
Fujitsu 4Mb 180nm ReRAM Test Collaborations

	NSWC Crane	NASA GSFC	NASA JPL
DPA			TEM complete; Memory organization similar to Panasonic
TID	Failure between 20 and 50 krad (Si) No bit corruption observed; likely peripheral CMOS failure. Similar results at GSFC & NSWC Crane.		
Heavy Ion		No SEU; SEFI LET_{th} < 5.6 $MeVcm^2/mg$ One device failure at LET 5.6, cause TBD	
Proton		200 MeV: No SEU; SEFI CS ~$2x10^{-11}cm^2$	
Reliability			Electrical and temperature stressing in progress

Fujitsu ReRAM (Memory Array)



Panasonic Embedded ReRAM

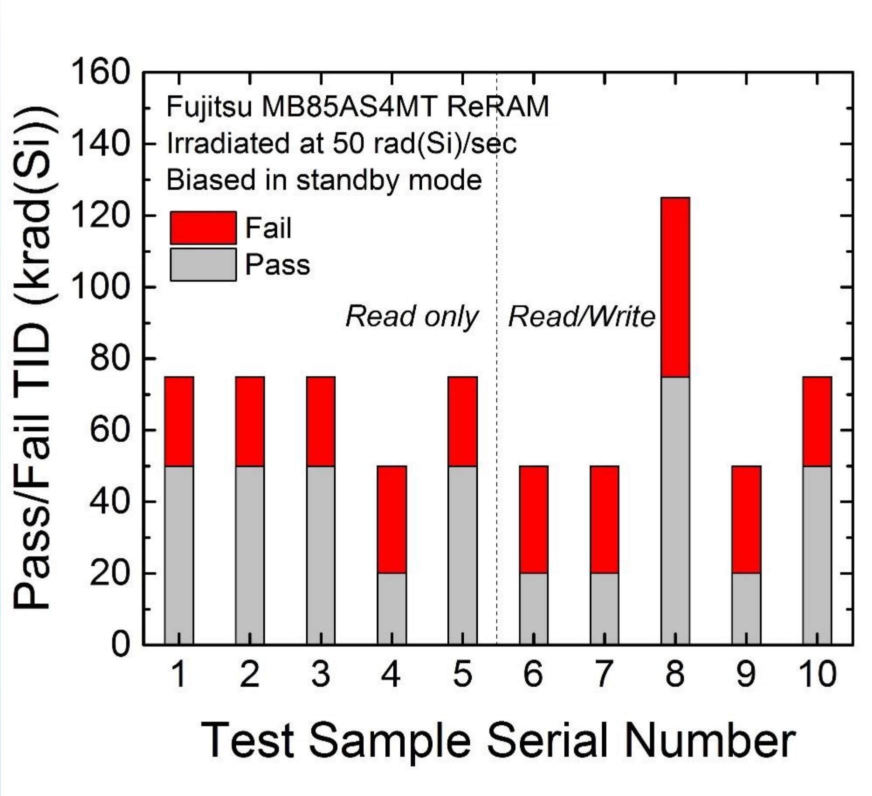


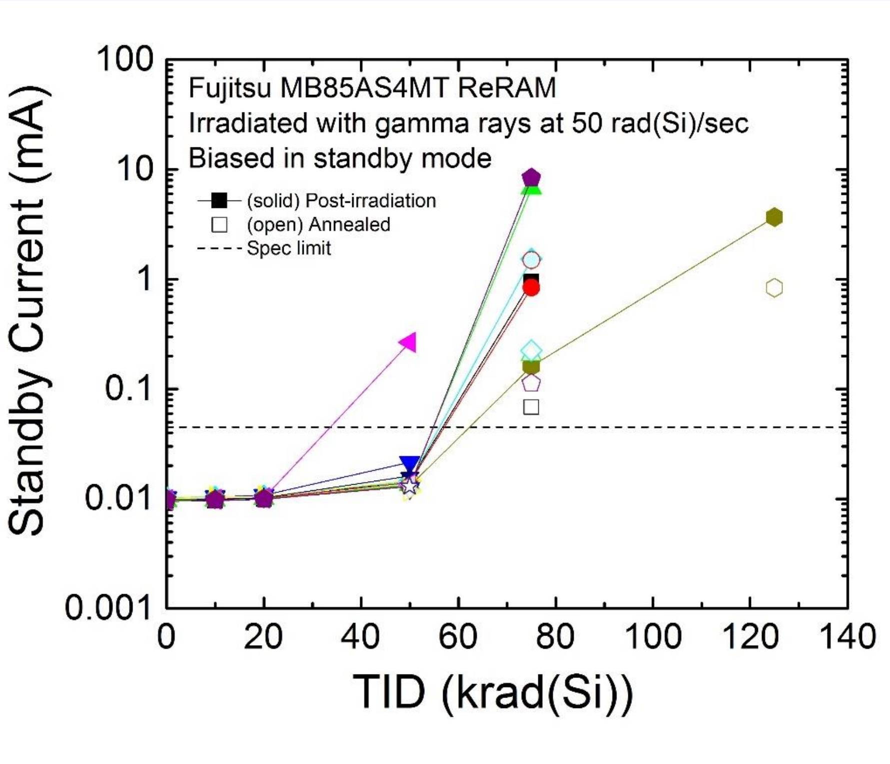
Fujitsu ReRAM

- **Memory Array TEM for the Fujitsu chip shows the identical memory layout and feature size as the Panasonic Microcontroller ReRAM**
- **Memory element located between 3rd and 4th metal paired with transistor below for a 1T1R bit cell**
- **Expect intrinsic reliability performance to be similar**
  - **3E7 endurance tested on 256Bytes with no read errors with EDAC**
  - **EDAC cannot be turned off so will see no failures until overwhelmed**

Fujitsu ReRAM (TID)

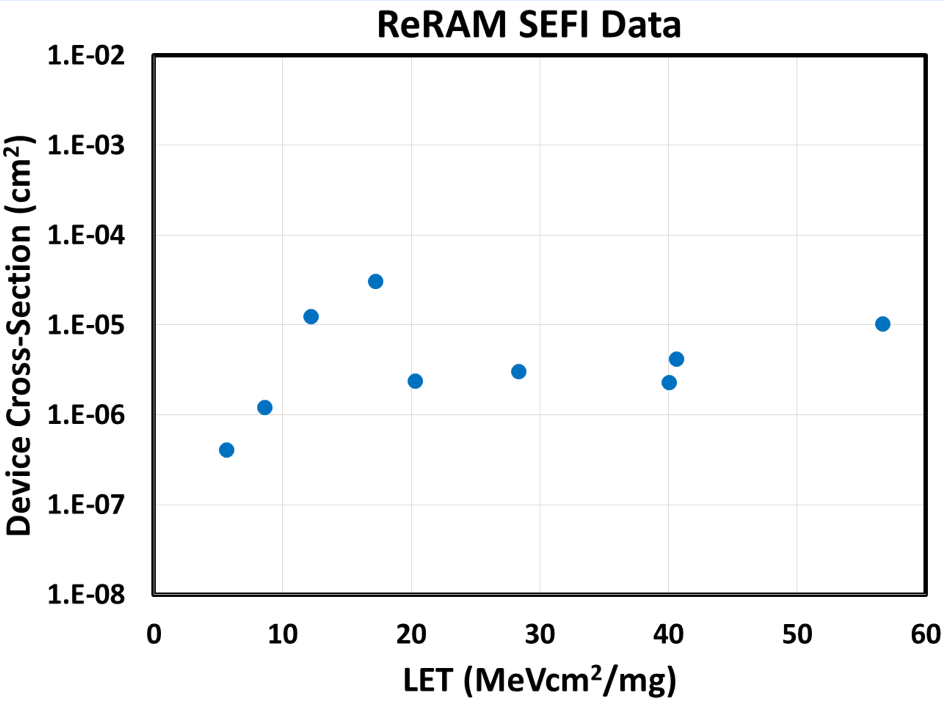
- **No indication of data corruption during TID test**
- **Communication with device began failing after 20 krad (Si) step (SPI interface no longer responsive)**

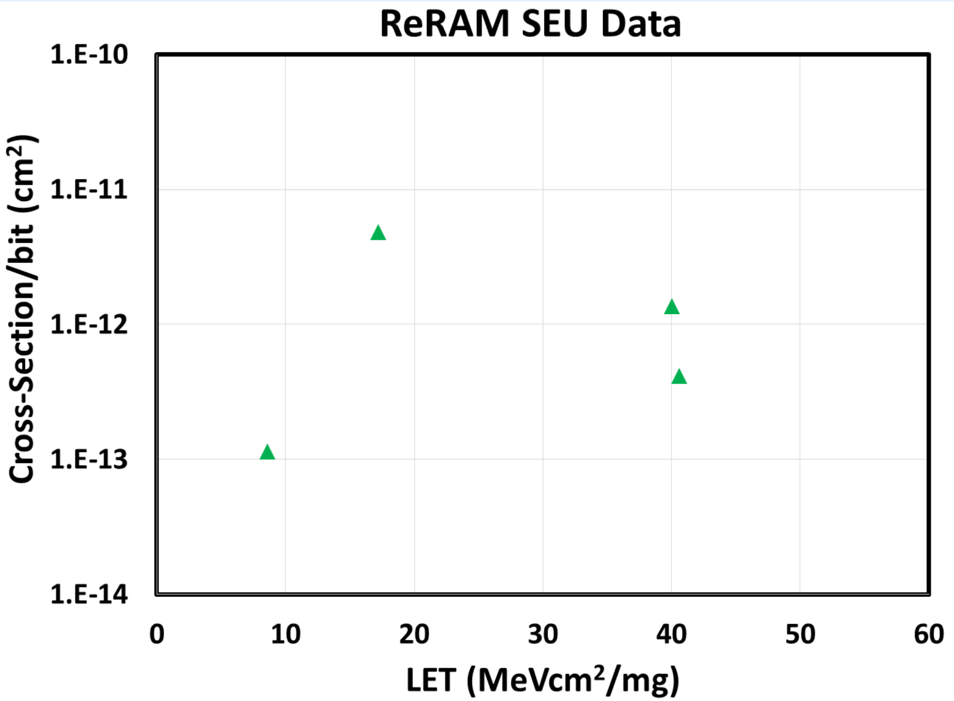




Fujitsu ReRAM (HI)

- No SEU observed during static irradiations up to LET of 56.6 MeV*cm^2/mg.
- SEFI observed at lowest LET tested (5.6)
- Single errors noted after four dynamic runs
- Two devices permanently damaged (LET 40 and LET 5.6)



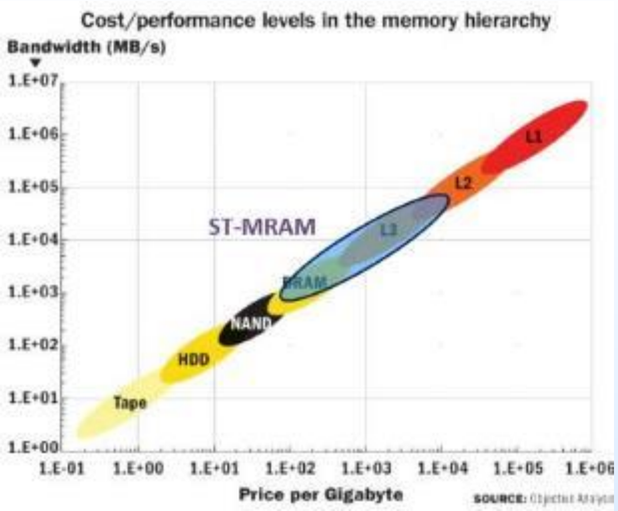


Fujitsu ReRAM Summary

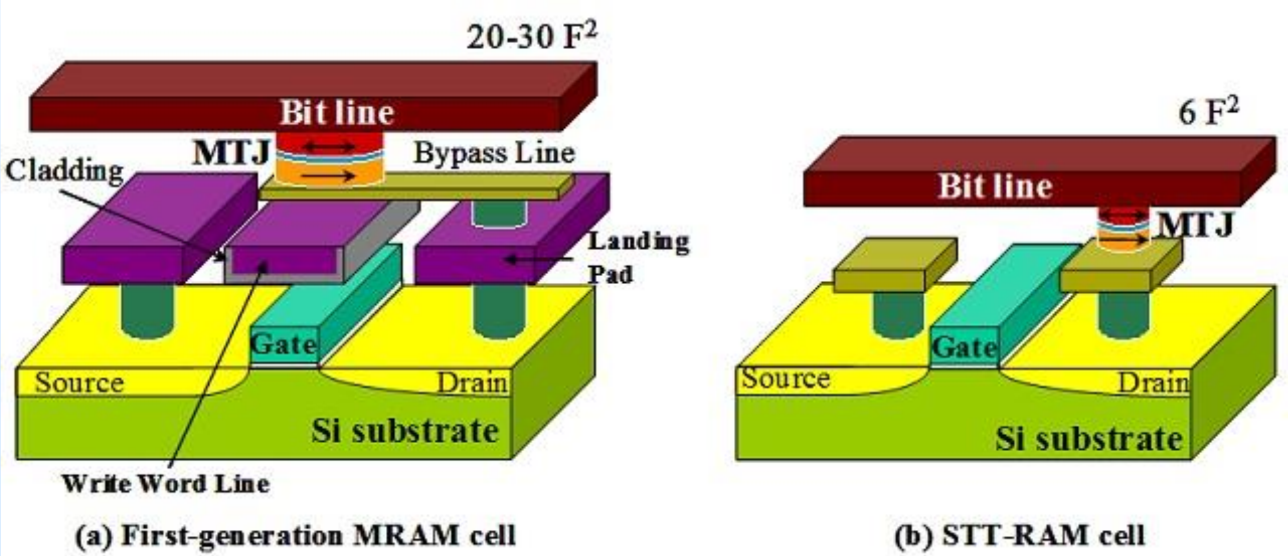
- **Stand alone chip with higher density for study comparison without microcontroller**
- **TID, HI, and proton testing do not show indications of data errors**
- **SEFI cross section for HI similar to the Panasonic embedded ReRAM**
- **Endurance reliability is significantly higher with EDAC but we will not see errors until EDAC is overwhelmed**
- **Resistive memory is still low density but has plans for density scaling for potential storage memory use**

Spin Torque Transfer Magnetic Memory (STT-MRAM)

- **STT-MRAM is a near term storage & working memory technology**
  - **MRAM already used in RH applications**
  - **MRAM can be used as (RH) system memory or storage memory replacing DRAM or NAND**



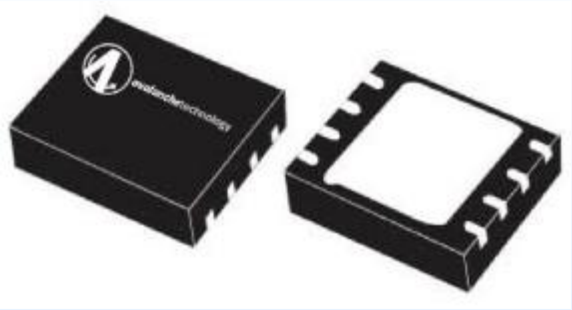
- **STT-MRAM enables further scaling of density well above current RH**



(a) First-generation MRAM cell
(b) STT-RAM cell

Spin Torque Transfer Magnetic Memory (STT-MRAM)

- **Avalanche Technology**
  - **1st Gen MRAM product "SPnvSRAM"**
  - **4Mb, 8Mb targeting high endurance, high data retention applications**
  - **Initial heavy-ion data in. Production chip STT-MRAM testing scheduled for FY17E/FY18B**
  - **Of interest to us for RH non-volatile memory uses**



- **Everspin Technologies**
  - **1st Gen MRAM in 16Mb products by Honeywell and Cobham**
  - **New STT-MRAM *256Mb DDR3* chip targeting high speed and high density**
  - **Testing scheduled for STMD for FY17E**
  - **Of interest for RH processor system memory**

9 x 13 BGA Package

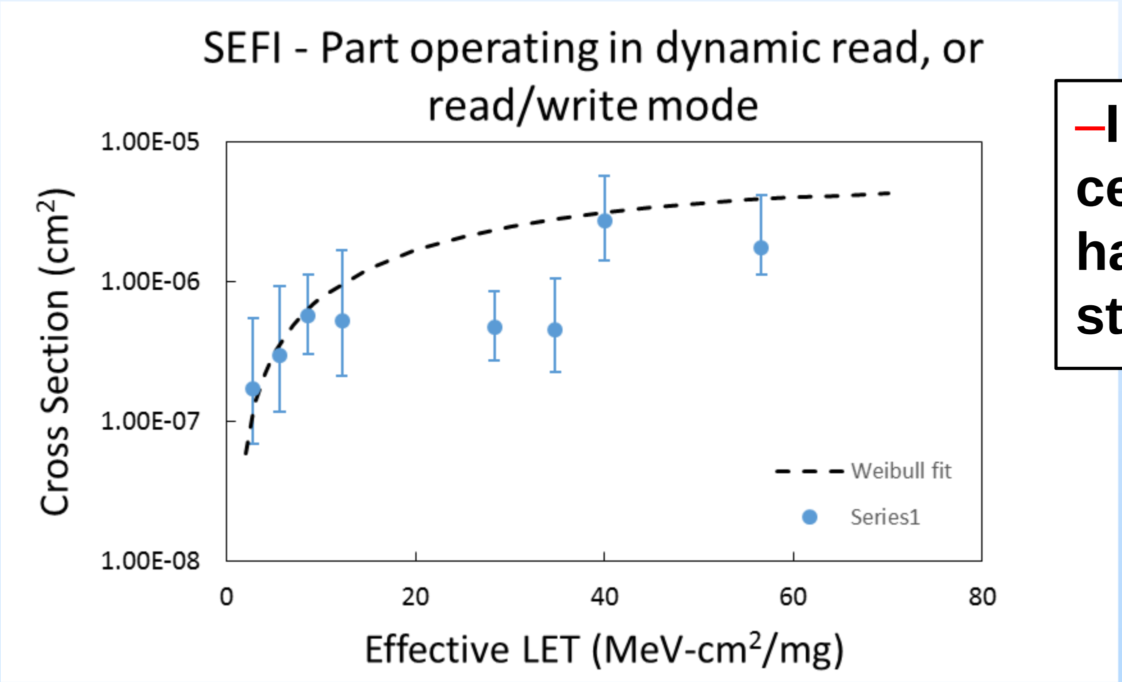
Avalanche STT-MRAM Test Collaborations

	NSWC Crane	NASA GSFC	NASA JPL
DPA			
TID		Late 2017	
Heavy Ion		No SEU; SEFI $LET_{th} < 2.8$ $MeVcm^2/mg$	
Laser		Late 2017	
Proton		200 MeV: No SEU; SEFI CS $1.24 \times 10^{-11} cm^2$	
Reliability			

Many remaining data gaps →pending additional parts for all parties!

Avalanche STT-MRAM (HI)

- **No SEU observed during static, unpowered runs**
- **Some data corruption (in large blocks) after dynamic modes due to un-commanded write operations**



–Individual bit cells are very hard, but SEFI still present

Avalanche STT-MRAM (Proton)

- Three runs conducted with 200 MeV Protons:
- Static, Powered On: No SEU noted in memory after 1.14×10^{11} p/cm^2 static irradiation
- Dynamic Read Only: A single SEFI after 8×10^{10} p/cm^2 fully recoverable with power cycle.
- Dynamic Read & Write: A single SEFI after 7×10^{10} p/cm^2. Functionality recovered with power cycle, but two blocks (32KB) of memory no longer programmable (total 15.5 krad(Si))

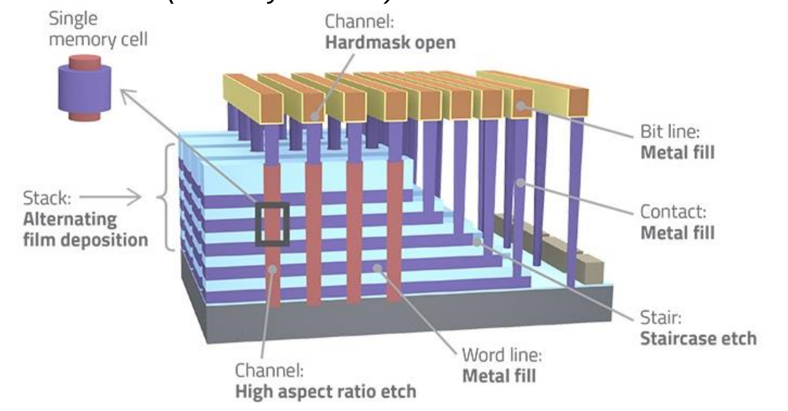
Avalanche STT-MRAM Summary

- Very limited HI and proton testing show no memory errors and some SEFI
- More chips from Avalanche needed for more complete SEE testing as well as TID and reliability

3D SLC/MLC/TLC NAND Flash

- **NAND Flash moving to 3D structures**
  - Over 50% of NAND produced today
  - By 2020 over 90% will be 3D
  - Actual feature size is ~50nm
  - Scaling will be by inc. # of stacks

3D NAND Layout (courtesy of LAM)



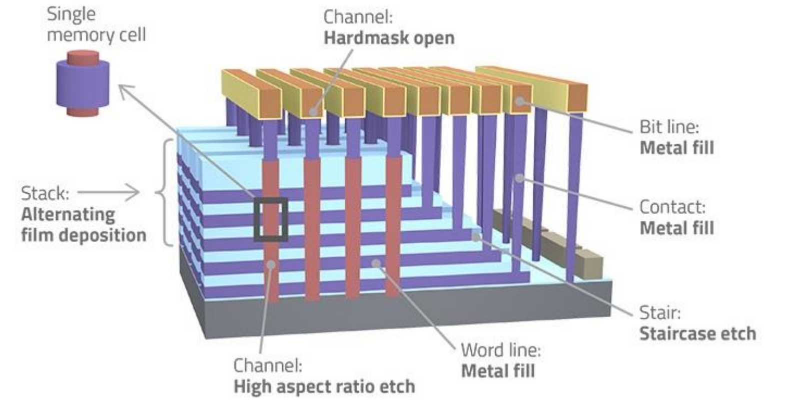
- **Massive density**
  - Complex radiation/reliability tests
  - With MLC and TLC come higher built-in EDAC requirements
  - Micron producing 6Tb LBGA chips
  - Impractical to test entire addr space
- **Secondary concerns:**
  - Harder to acquire discrete devices as SSD market consumes all (few users of individual 1Tb+ chips!)
  - Rapid development / production / obsolescence cycle is not ideal for mil/aero COTS applications

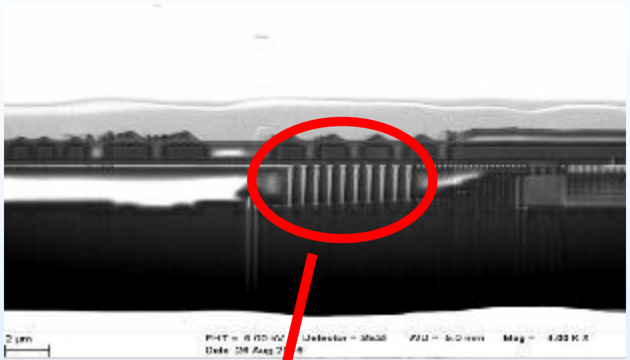
Hynix 3D NAND Flash Collaborations

	NSWC Crane	NASA GSFC	NASA JPL
DPA	Completed: X-ray, die markings, FIB, SEM		Completed: Bit Cell Analysis, Comparisons to VNAND
TID	In Progress		
Heavy Ion		MLC SEU: $LET_{th} < 3.5$ SLC SEU: $3.5 < LET_{th} < 7$ SEFI: $LET_{th} < 3.5$ Destructive: $35 < LET_{th} < 86$ *Inverse fluence dependence in MLC mode observed *Low MBU rate compared to 16nm planar, roll dependence observed	
Laser		Plans TBD: Identify sources of SEFI	
Proton		60/200 MeV Proton: MLC SEU CS: $1x10^{-14}cm^2/bit$ SLC SEU CS: $2.5x10^{-18}cm^2/bit$ 200 MeV SEFI CS: $\sim 1x10^{-11}cm^2$	
Reliability			Complete: Endurance (fail at 50k prog/erase cycles) Electrical and temperature stressing on going

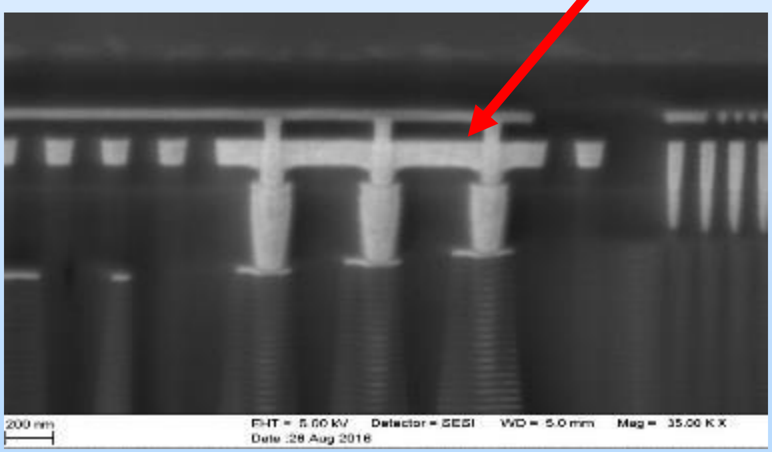
Hynix 3D 1X nm NAND equivalent FIB Cross-Section- 128Gb

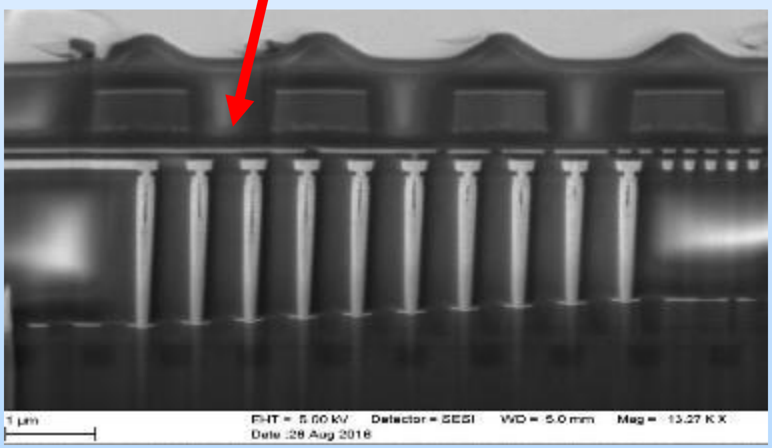
3D NAND Layout (courtesy of LAM)





Cross section showing FLASH array transition to periphery. Connections are identified for reference to higher magnification images below. Cross sections were taken along the Y-Axis

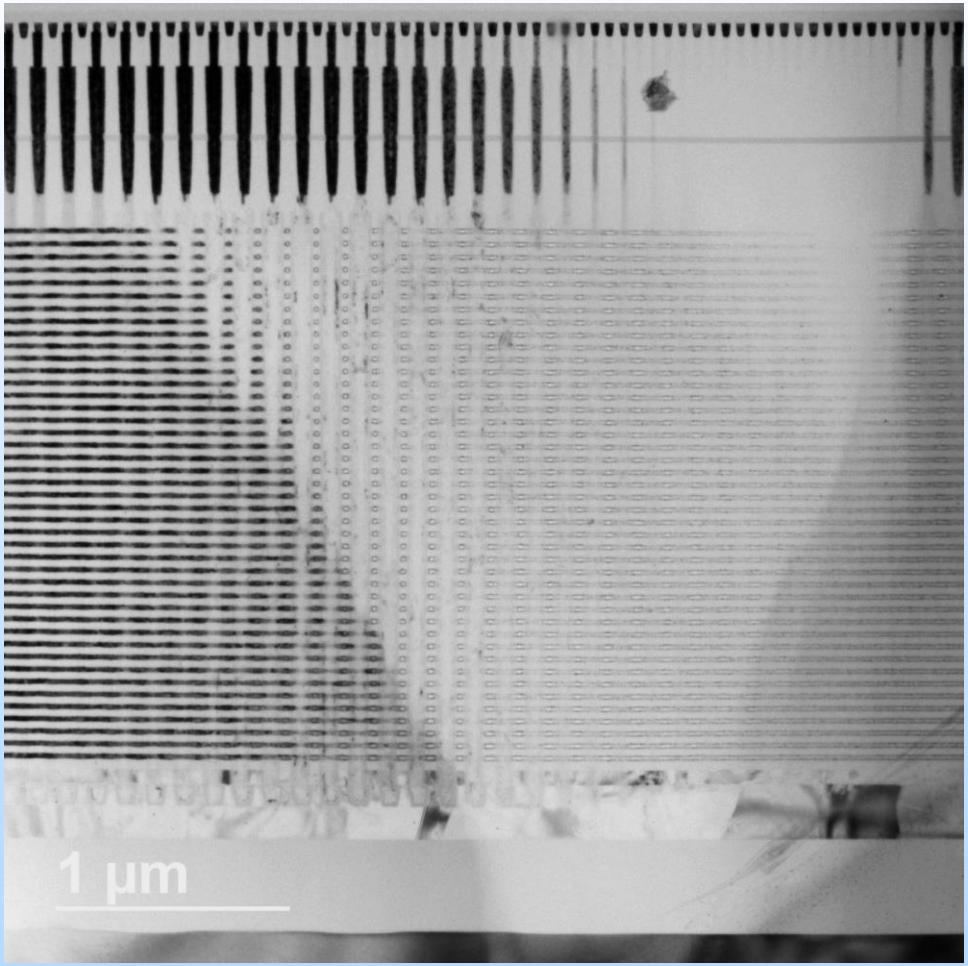


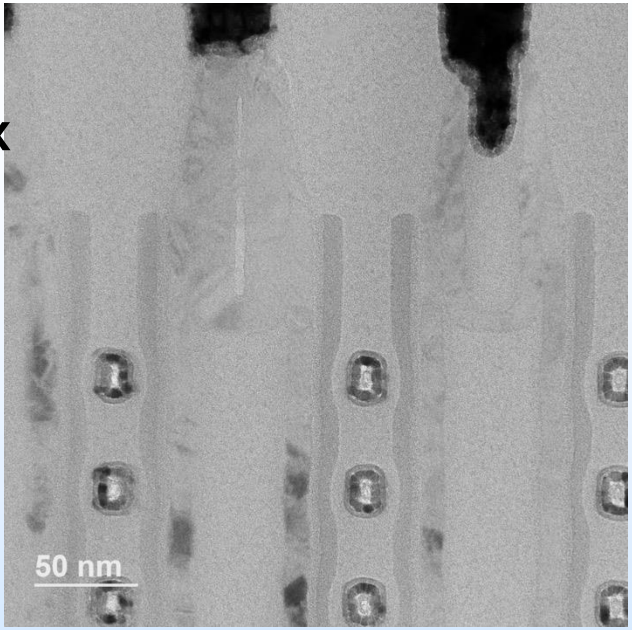


Higher magnification images of array connections

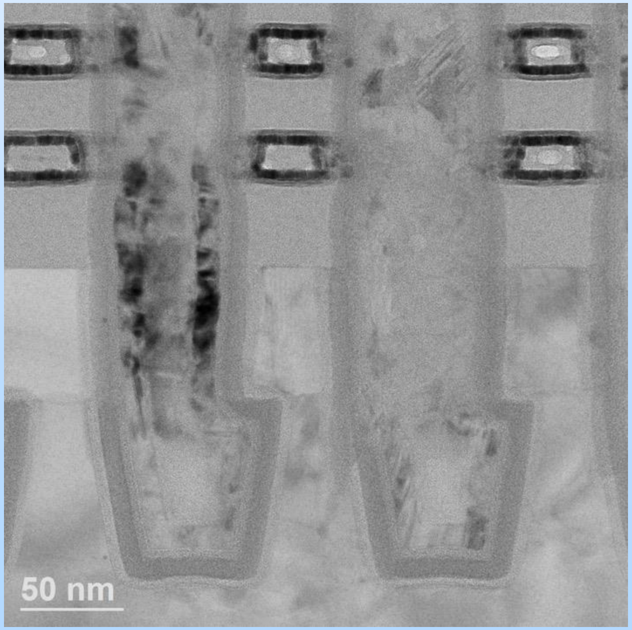
Hynix 3D NAND (128Gb, MLC) initial construction SEM analysis reveals a single die with 3D construction comprising of 40 physical device layers and staircase array edge connection.

Overview of the Vertical Stack @ 4500x





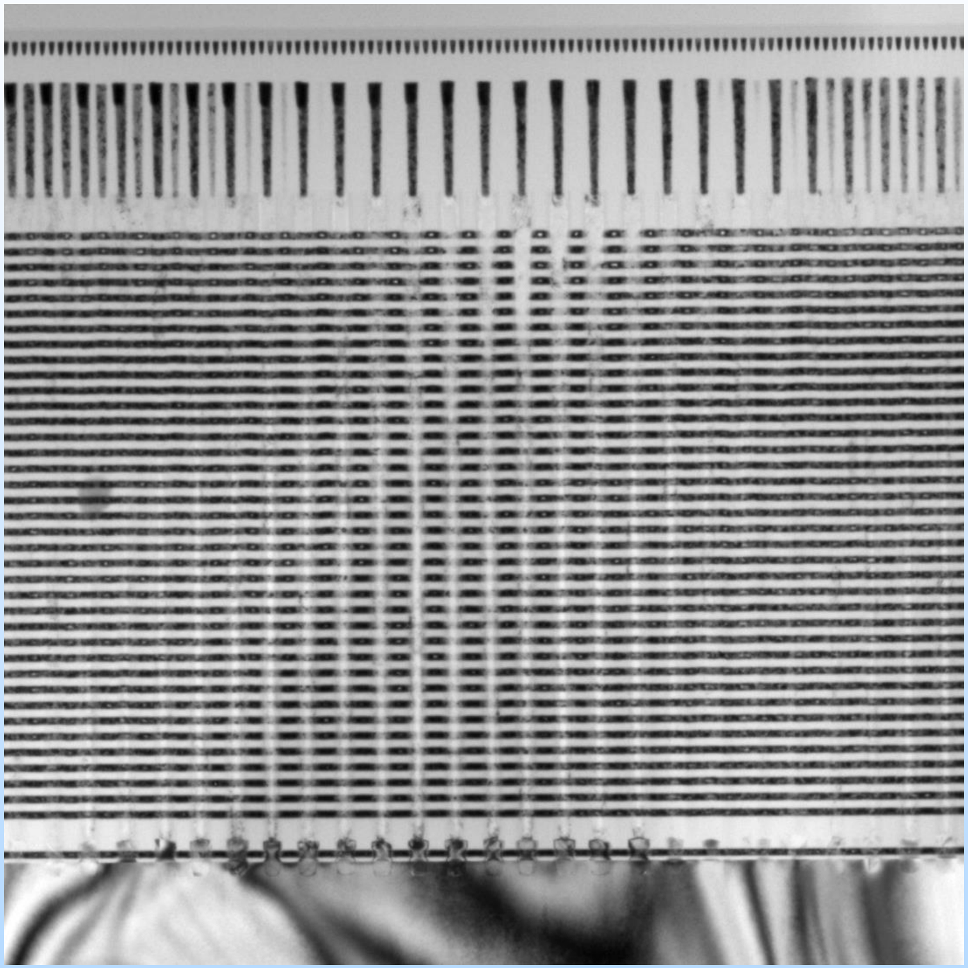
Detail View
Top of Array

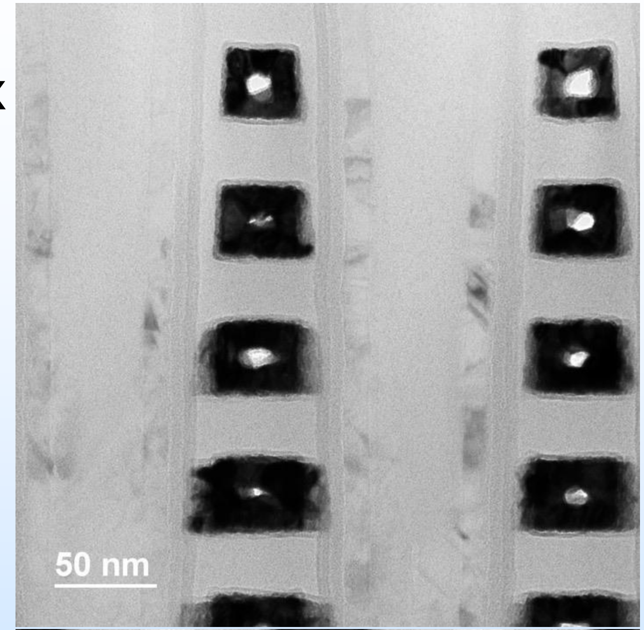


Detail View
Bottom
of Array

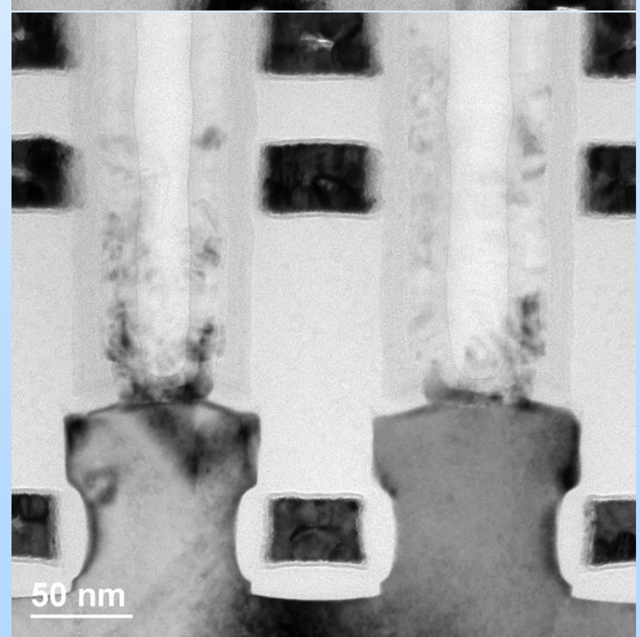
Samsung VNAND 2014
Y Direction Top and Bottom Details

Overview of the Vertical Stack @ 4500x





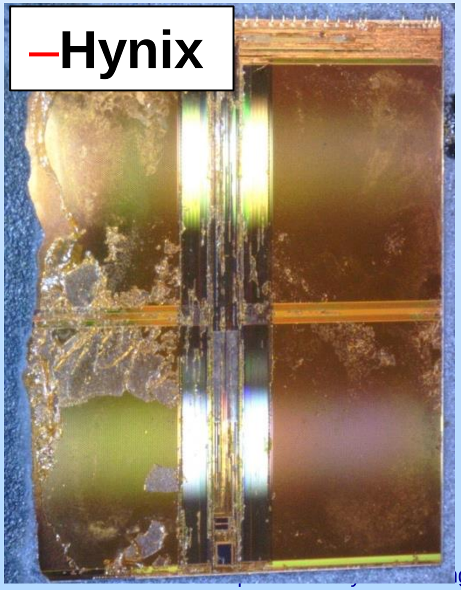
Detail View
Top of Array

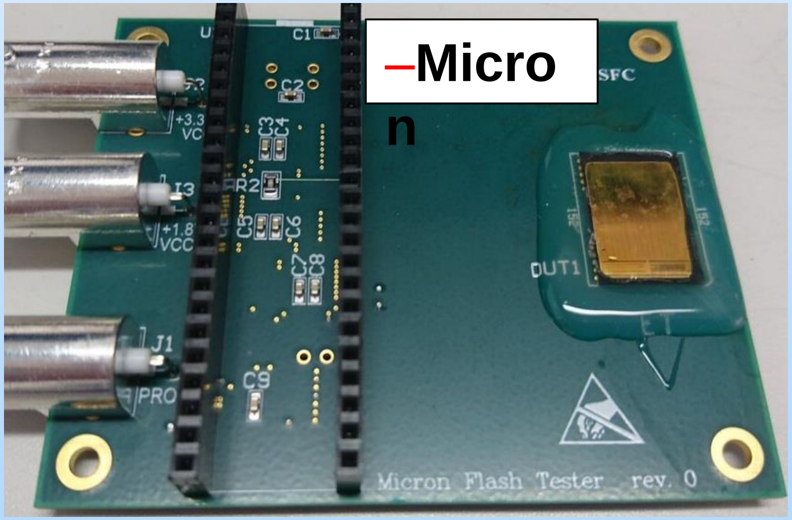


**Detail View
Bottom
of Array**

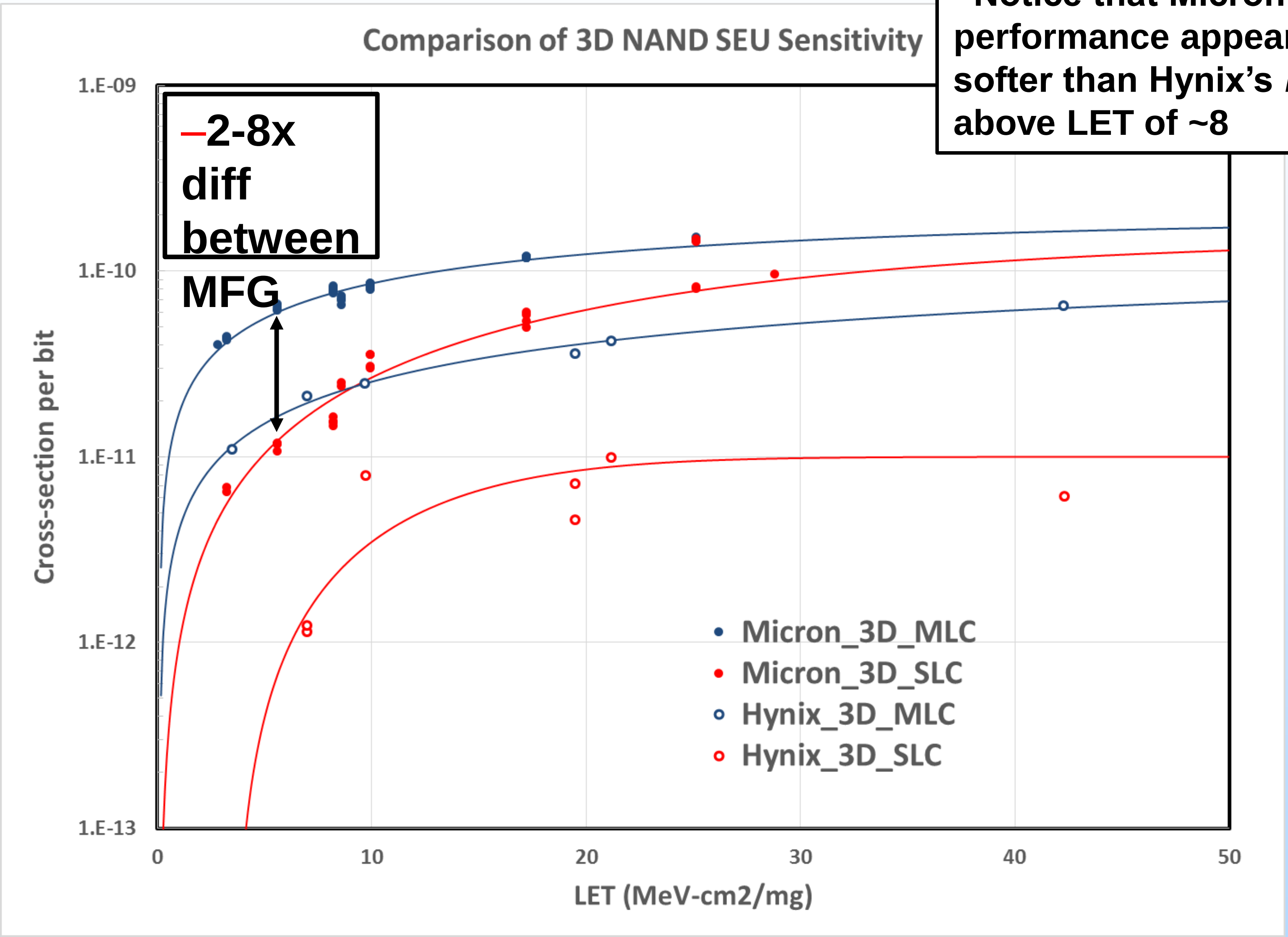
Comparison of 3D NAND Flash Tech

- **Hynix 3D NAND (H27QDG822C8R-BCG)**
  - **Single die, MLC with SLC mode, 1x128Gb, charge trapping**
- **Micron 3D NAND (MT29F1T08CMHBBJ4)**
  - **Stacked die, MLC with SLC mode, 4x256Gb, floating gate**
- **Full data set tested for Hynix**
- **Limited data so far for Micron (static SEU only)**





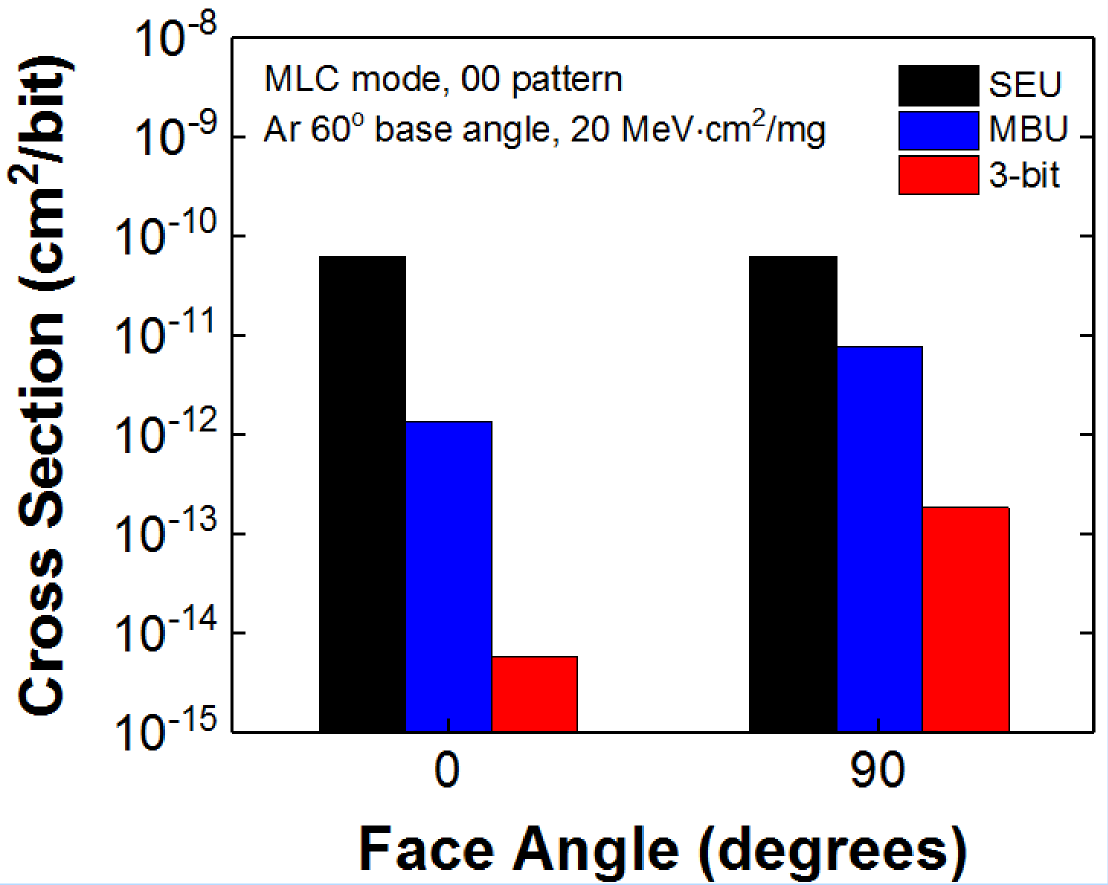
3D NAND Static SEU Comparison:



– Notice that Micron's *SLC* performance appears softer than Hynix's *MLC* above LET of ~8

Hynix 3D NAND Flash (HI)

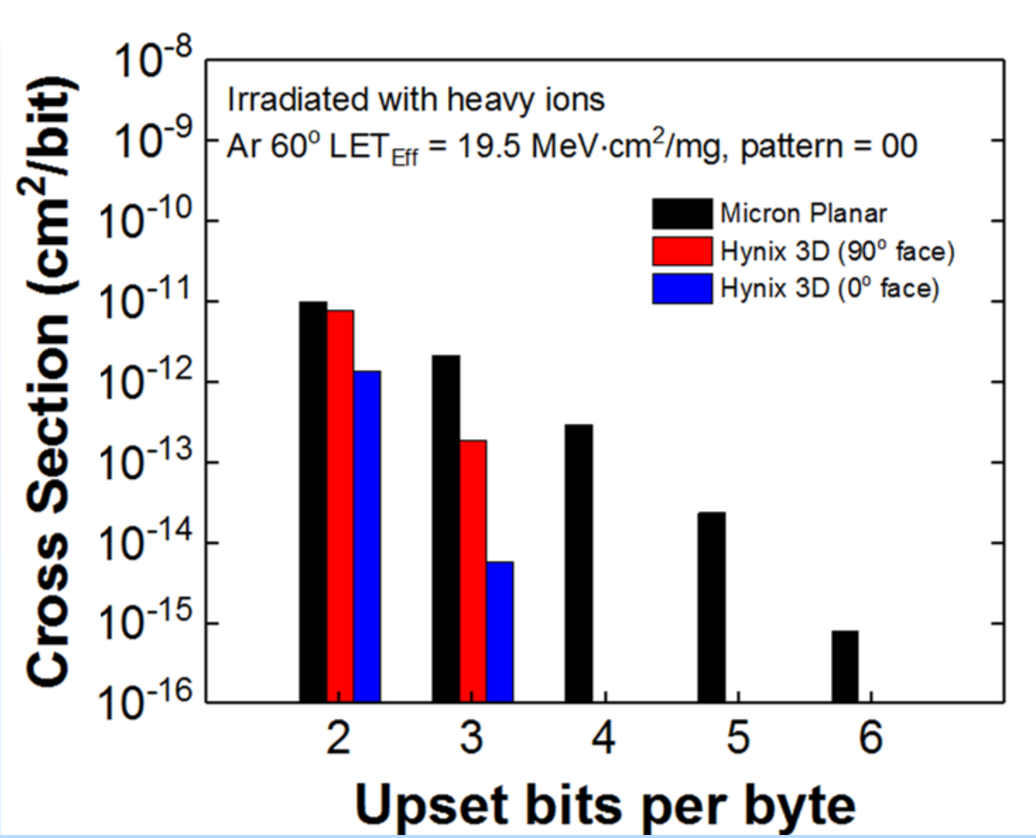
- **First tests of 3D NAND Flash**
  - **Explored MBU dependence on direction of irradiation:**



– **For fixed incidence angle of 60 degrees, the direction of irradiation affected MBU rate**

Hynix 3D NAND Flash (HI)

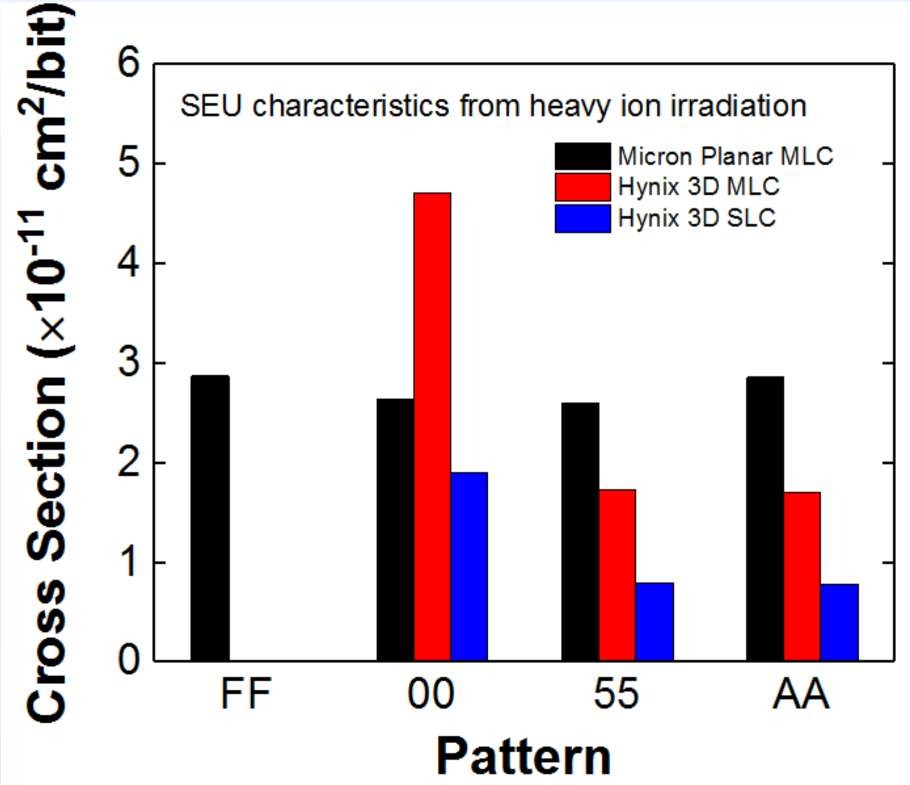
- **Data compared to Micron 16nm planar NAND Flash (also 128Gb and MLC)**



– **Fewer MBUs observed, and none longer than 3 bits/byte**

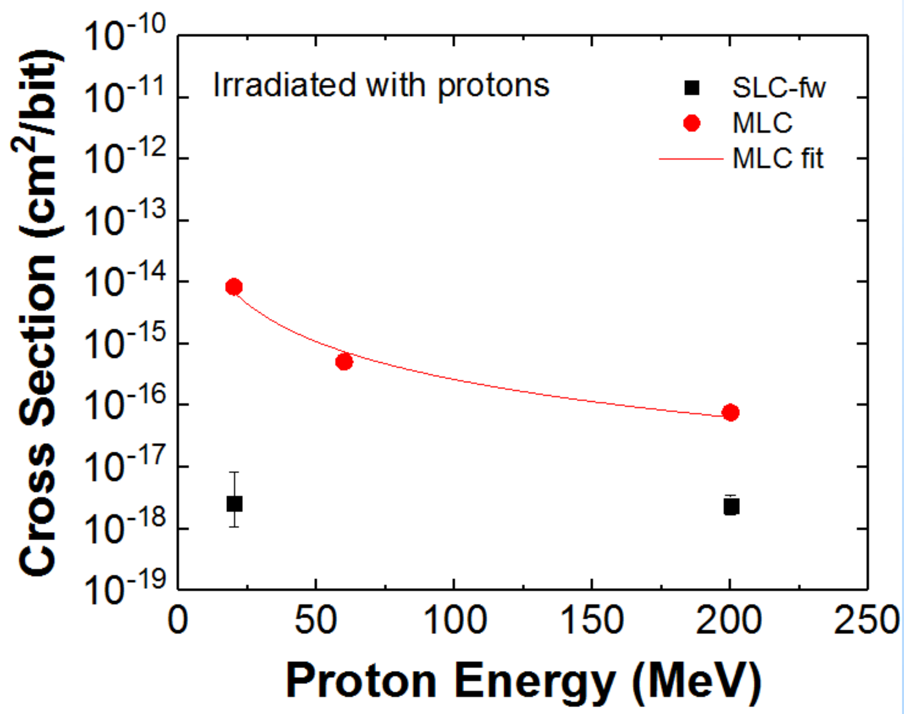
Hynix NAND Flash (HI)

- **A strong pattern dependence was observed with Hynix 3D NAND. Erased (logic HIGH) bits can not be upset. Micron 16nm planar (and preliminarily, 3D NAND) has no pattern dependence).**



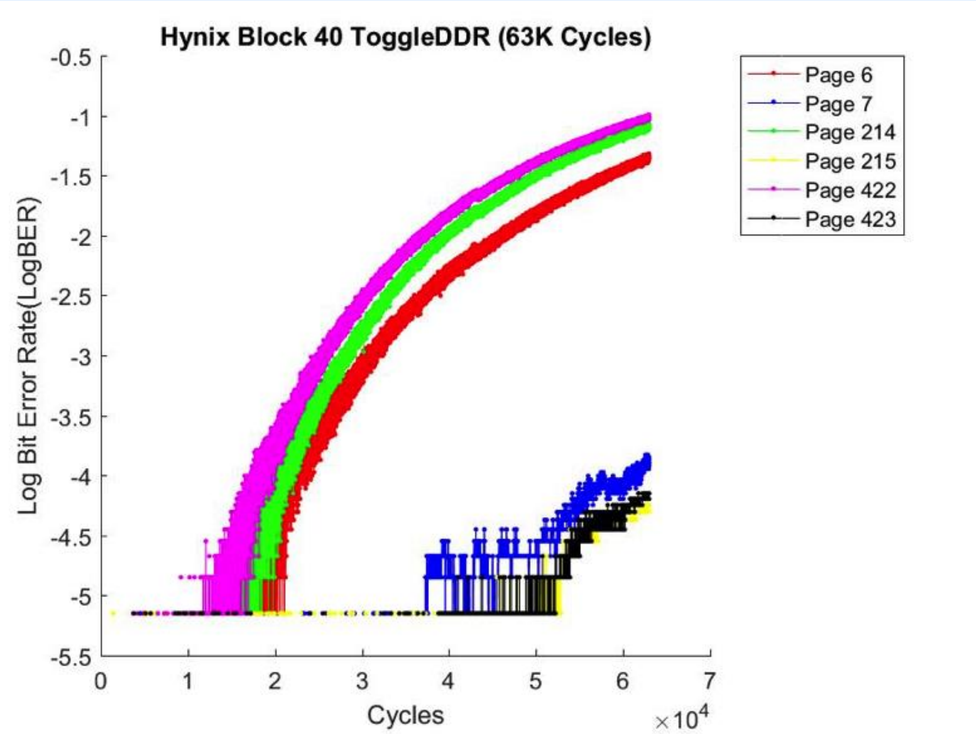
Hynix 3D NAND Flash (Proton)

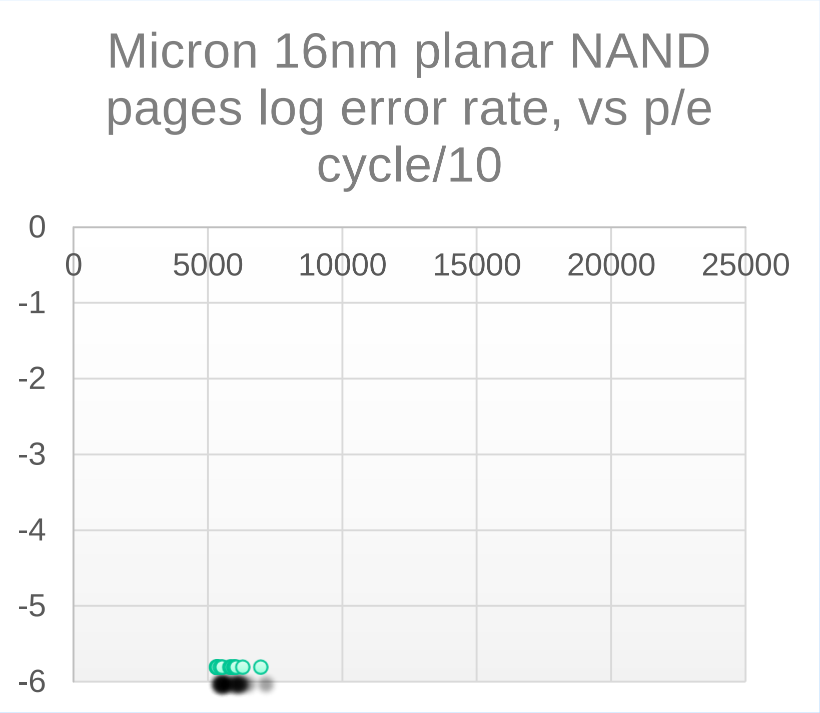
- **Devices were irradiated with multiple proton energies at Massachusetts General Hospital.**
- **Same pattern dependence (only 0 -> 1 errors)**
- **Two SEFI observed, CS ~ $5.8\times10^{-11}/cm^2$ at 60 MeV and $1.1\times10^{-11}/cm^2$ at 200 MeV**



Hynix 3D NAND

- **Program/Erase Endurance**
  - **Fails at 50-60K writes due to erase failure vs ~250K cycles for Micron 16nm planar NAND was still functional**
  - **Upper pages (even pages, second bit in the MLC) have significantly higher error rate**





3DNAND Hynix Summary

- Wafer level 3D structures with ~50nm feature size
- For static SEU, Hynix 3DNAND has 2-8x lower cross section per bit than Micron 3DNAND
- Lots of interesting results in these first tests of the Hynix 3DNAND
  - For fixed incidence angle see MBU rate change as function of irradiation angle
  - No >3bit/byte MBUs as compared to 16nm 2D NAND (could be due to feature size)
  - HI and proton tests both show very strong pattern dependence (only 0 -> 1 errors) potentially simplifying error correction
- Endurance reliability well above specification but prone to catastrophic failure at ~50K writes

Upcoming Radiation Tests

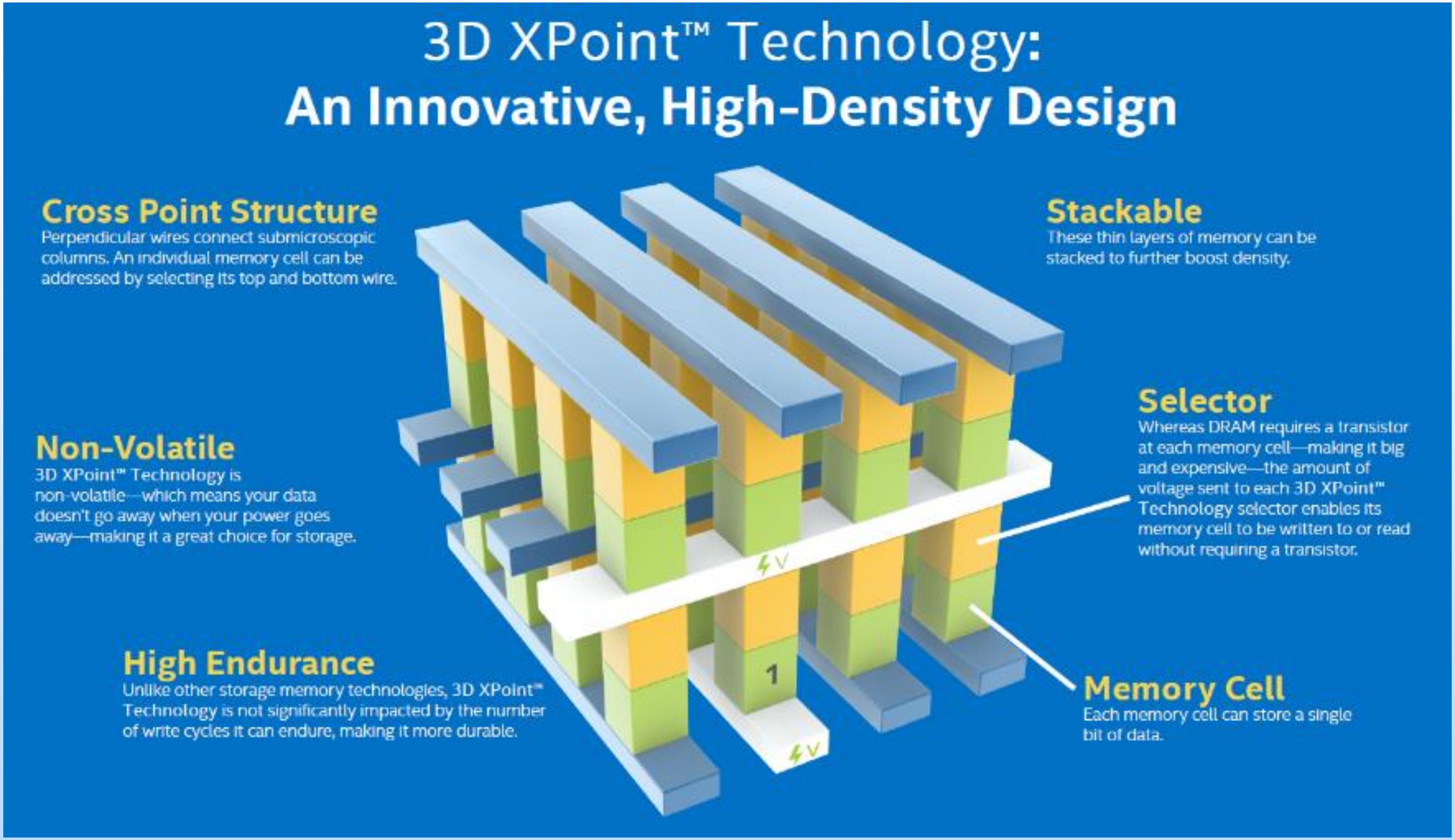
	Manufacturer	Technology	Device Description	Plans
Coming Soon	Micron	3D NAND, MLC/SLC	256Gb NAND Flash	Heavy Ion: June 2017 Investigate fluence dependence on MLC operation and roll/tilt angular effects on 3D/MLC structures
	Intel	Optane (3D Xpoint)	16GB PCIe SSD	Proton: Fall 2017 First look at new technology
Future Interest	Avalanche	STT-MRAM	Production version, serial memory	Expand on initial data with larger quantity of production parts
	Everspin	STT-MRAM	DDR3-interface high-speed NVM	Coordinate with NEPP DDR task!
	Any	Advanced 2D/3D NAND	NAND Flash Memory	Continued TID/SEE Testing
	Any future NVM of relevance to mil/aero community… samples always welcome!			

Future Objectives

- **Enhance collaboration with NASA STMD and Navy Crane**
- **Continue to track and test new NVM products and technologies for radiation *and* reliability**
- **Collaborate with NEPP DDR/SDRAM task as technologies promise to "bridge the gap" between system memory and storage memory**
- **Provide data analytics – radiation/reliability trends versus**
  - **CMOS nodes, manufacturers, etc..**
  - **Architecture (SLC, MLC, TLC)**
  - **Planar - vertical (3D), etc…**
- **Update NEPP test guidelines**

https://nepp.nasa.gov

1st Device's Ordered: Intel Optane™



Diatribe: Gartner Hype Cycle Concept